

Department of Electronics & Telecommunication Engineering

Vision of the Institute

Empowerment Through Knowledge

Mission of the Institute

Developing human potential to serve the nation by

- *Dedicated efforts for quality Education*
- *Yearning to promote research and development.*
- *Persistent endeavor to imbibe moral and professional ethics.*
- *Inculcating the concept of emotional intelligence.*
- *Emphasizing extension work to reach out to the society.*
- *Treading the path to meet the future challenges*

Department of Electronics & Telecommunication Engineering

Vision of the Department

To be a distinct department building globally competent Electronics and Telecommunication professionals

Mission of the Department

- *Nurturing the spirit of innovation & creativity by providing conducive learning*
- *Enhancing potential of students to be globally competent by providing platform to build skills in advanced technologies and inculcate life-long learning*
- *Enabling students to imbibe social as well as ethical values as inner strength through educational experiences and collaborations*

Department of Electronics & Telecommunication Engineering

Programme Educational Objectives (PEOs)

PEO1:

Possess strong basics of science and engineering as well as critical problem skills to innovate and solve real-life engineering problems.

PEO2:

Acquire technical competency in Electronics & Telecommunication field leading to higher studies, career/technical profession and

PEO3:

Exhibit proficiency in constantly evolving multidisciplinary approach and conduct themselves in professional and ethical manner at all levels.

PEO4:

Demonstrate attributes for need based learning and utilize their engineering skills along with effective communication skills and spirit of team work in social context

Department of Electronics & Telecommunication Engineering

Programme Specific Outcomes (PSOs)

PSO1:

Identify the problem and creat a solution relevant to Electronics & Telecommunication Engineering.

PSO2:

Act effectively, ethically and responsibly to tackle societal and environmental issues related to Electronics & Telecommunication Engineering.

PSO3:

Upgrade to the latest trends and accept the advancement of the technologies in the field of Electronics & Telecommunication Engineering.

Department of Electronics & Telecommunication Engineering

Programme Outcomes (POs)

PO1	Engineering Knowledge	Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	Problem Analysis	Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	Design & Development of Solutions	Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	Conduct investigations of complex problems	Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	Modern Tools Usage	Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	The engineer and society	Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	Environment & Sustainability	Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	Ethics	Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	Individual & Team work	Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	Communication	Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	Project management & Finance	Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments
PO12	Lifelong Learning	Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change

Academic Year: 2023-2024, Semester: I

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Experiment No. 1

CO Addressed: CO2- Understand and explain various digital modulation techniques used in digital communication systems and analyze their performance in presence of AWGN noise.

AIM :-

To modulate and demodulate BPSK & its spectral analysis (DSO)

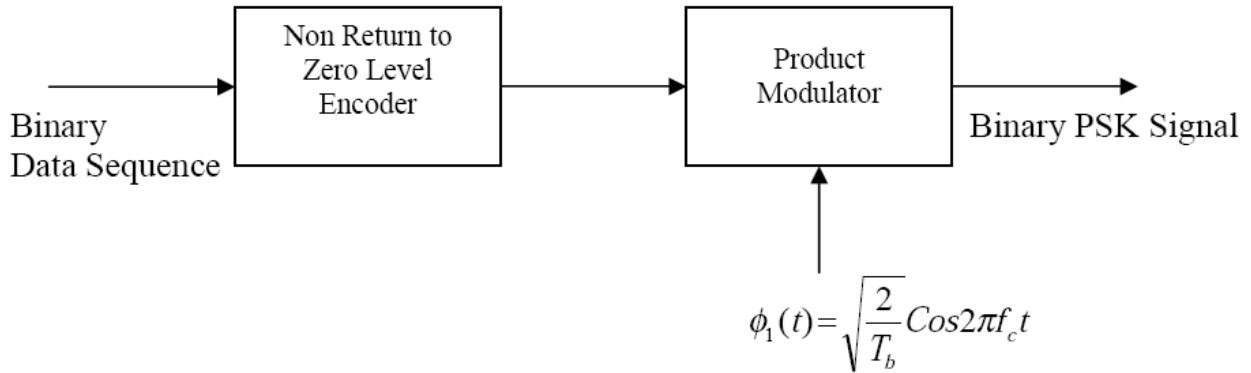
EQUIPMENT: - BPSK modem, DSO, connecting wires, probes.

THEORY:-

In binary PSK the transmitted signal is a sinusoidal of fixed amplitude. It has one fixed phase when the data is at one level & when the data is at the other level the phase is differ by 180. In this kit we have derived a sinusoid from a crystal clock using IC4017's & frequency divider & 2nd order butter worth filter & for phase shifted wave form we have used OP-AMP Inverter.

Also two different bit patterns are also derived from a basis clock. For transmitter section we have used IC 4052 [analog switch].A sinusoid & phase shifted sinusoid are two I/P's to Analog switch & bit pattern is connected to control I/P of 4052.O/P of 4052 is a required BPSK output. Also for synchronization purpose a start signal (power on mono) is send. This signal is ORed with bit pattern & then given to transmitter. At the receiver we have to derive carrier frequency from BPSK waveform. So this waveform is given to squaring the circuit (IC1496 multiplier). At the O/P of 1496 we have 2 fc frequencies. By using Band pass filter with center frequency '2fc & frequency divider (division factor 2). We get carrier frequency. For detection of data from BPSK signal, phase comparator section of PLL (IC565) is used. One I/P to PLL is BPSK signal & Other I/P is recovered carrier. O/P of PLL is then given to the filter. O/P of filter is either as digital data or inverted one. Then with the help of start signal we corrected the data. We know that at the 'Power on' we have send '1' as digital data. O/P of filter is latched at this instant. If it is '1' then we get correct data. If this is zero then O/P is inverted & therefore we get correct data.

Coherent Binary PSK:



Fig(a) Block diagram of BPSK transmitter

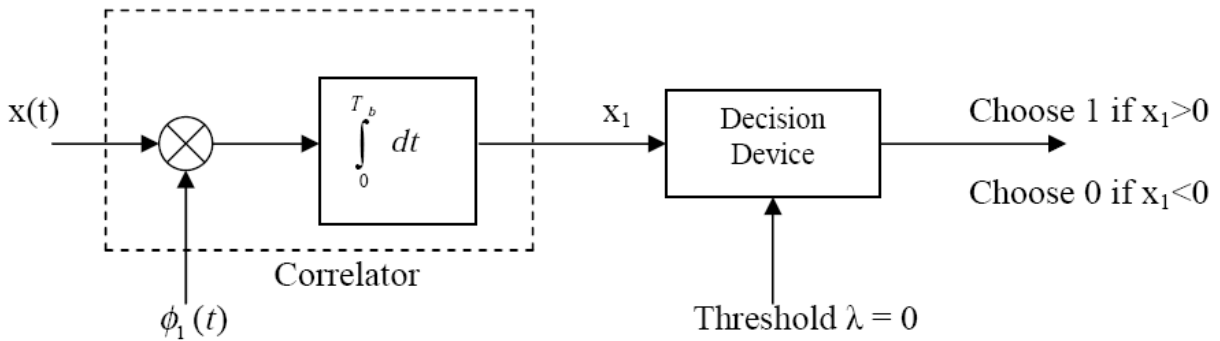


Fig (b) Coherent binary PSK receiver

In a Coherent binary PSK system the pair of signals $S_1(t)$ and $S_2(t)$ are used to represent binary symbol '1' and '0' respectively.

$$S_1(t) = \sqrt{\frac{2E_b}{T_b}} \cos 2\pi f_c t \quad \text{-----} \quad \text{for Symbol '1'}$$

$$S_2(t) = \sqrt{\frac{2E_b}{T_b}} \cos(2\pi f_c t + \pi) = -\sqrt{\frac{2E_b}{T_b}} \cos 2\pi f_c t \quad \text{-----} \quad \text{for Symbol '0'}$$

Where E_b = Average energy transmitted per bit $E_b = \frac{E_{b0} + E_{b1}}{2}$

In the case of PSK, there is only one basic function of Unit energy which is given by

$$\phi_1(t) = \sqrt{\frac{2}{T_b}} \cos 2\pi f_c t \quad 0 \leq t \leq T_b$$

Therefore the transmitted signals are given by

$$S_1(t) = \sqrt{E_b} \phi_1(t) \quad 0 \leq t \leq T_b \quad \text{for Symbol 1}$$

$$S_2(t) = -\sqrt{E_b} \phi_1(t) \quad 0 \leq t \leq T_b \quad \text{for Symbol 0}$$

A Coherent BPSK is characterized by having a signal space that is one dimensional (N=1) with two message points (M=2)

$$S_{11} = \int_0^{T_b} S_1(t) \phi_1(t) dt = +\sqrt{E_b}$$

$$S_{21} = \int_0^{T_b} S_2(t) \phi_1(t) dt = -\sqrt{E_b}$$

The message point corresponding to $S_1(t)$ is located at $S_{11} = +\sqrt{E_b}$ and $S_2(t)$ is located at $S_{21} = -\sqrt{E_b}$.

To generate a binary PSK signal we have to represent the input binary sequence in polar form with symbol '1' and '0' represented by constant amplitude levels of $+\sqrt{E_b}$ & $-\sqrt{E_b}$ respectively. This signal transmission encoding is performed by a NRZ level encoder. The resulting binary wave [in polar form] and a sinusoidal carrier $\phi_1(t)$ [whose frequency $f_c = \frac{n_c}{T_b}$] are applied to a product modulator. The desired BPSK wave is obtained at the modulator output.

To detect the original binary sequence of 1's and 0's we apply the noisy PSK signal $x(t)$ to a Correlator, which is also supplied with a locally generated coherent reference signal $\phi_1(t)$ as shown in fig (b). The correlator output x_1 is compared with a threshold of zero volt.

If $x_1 > 0$, the receiver decides in favour of symbol 1.

If $x_1 < 0$, the receiver decides in favour of symbol 0.

PROCEDURE:-

- 1] O/P of pattern Gen is connected to I/P of 'OR' Gate.
- 2] O/P of OR gate is connected to I/P of transmitter i.e. (i/p of MULT. Block).
- 3] O/P of 'MULT' Block i.e BPSK O/P is connected to I/P of 1496 Sq.cct.
- 4] O/P of 1496 Sq.cct is connected to I/P of Band Pass Filter.
- 5] O/P of Band Pass filter is connected to I/P of %2 N/W.
- 6] O/P of %2 N/W is connected to I/P of phase comparator.
- 7] BPSK O/P is connected to I/P 2 of phase comparator.
- 8] Observed signal at different test points together with I/P bit pattern.
- 9] Observed filter O/P & COMP. Block O/P. The O/P of COMP. Block is required detected O/P.

OBSERVATION TABLE:

Sr. No.	Name of Signal	Amplitude	Frequency

CONCLUSION:-

Staff Signature

Experiment No. 2

CO Addressed: CO2: Understand and explain various digital modulation techniques used in digital communication systems and analyze their performance in presence of AWGN noise.

AIM:

To study QPSK modulation and demodulation & its spectral analysis (DSO).

EQUIPMENT: QPSK modem, DSO, connecting wires, probes.

THEORY:

To transmit digital data on analog lines or even into space, modulation of analog signal is required. Simplest way is BPSK, where one phase of carrier is transmitted for '1' and inverted carrier is transmitted for digital '0'. Here if bit rate is ' T_b ' then bandwidth required is ' $2T_b$ '. To reduce this bandwidth requirement QPSK can be used. For QPSK bandwidth is ' T_b ' i.e half that of BPSK.

QPSK techniques come under carrier modulation type. Here i/p to the transmitter is digital data, in between processing is in analog form & finally o/p of receiver is again digital data same as fed to transmitter.

'Q' in 'QPSK' means quadrature i.e 4 four phases of carrier are transmitted depending upon bit pattern. Incoming bit pattern is divided into ODD & EVEN bit patterns. Odd pattern is multiplied by sine wave, & even wave is multiplied by cos wave. Sine & cos waves are 90 degree phase shifted. Now resulting two PSKs are added & we get vector addition o/p i.e if both bit is '1' we get 45 degree phase shifted carrier. If odd bit is 1 and even bit is 0 we get 135 degree phase carrier. If odd bit is 0 & even also 0 we get 225 degree. If odd bit is 0 & even bit is 1 we get 315 degree.

In QPSK, two consecutive bits are stored & for resulting four combinations (4) different phases of carrier are transmitted. By using 'D' flip-flop type arrangement incoming bit pattern is divided into two bit patterns viz. odd & even pattern, for obtaining this, basic clock whose frequency is ' f_b ' is divided by two, resulting odd & even clock frequencies are ' $f_b/2$ ' & they are complementary. Each bit is stored for ' $2T_b$ ' & even bit pattern will have bit no 2, 4, 6, etc stored for ' $2T_b$ '.

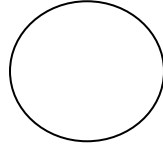
Here active edges of, odd & even clocks are separated by time ' T_b '. So out of two bits only one bit is changing after each ' T_b ' period but every bit is there for $2T_b$ time; so in this offset QPSK system every time phase changes by 90 degree only.

At receiver carrier is recovered from QPSK signal itself. This is synchronous reception. To recover carrier QPSK signal is raised to power four using analog multiplier. Then resulting signal is passed through bandpass filter whose center frequency is adjusted to 4 times carrier frequency. Then o/p of bandpass filter is divided by 4 to get carrier frequency. In this kit IC 1496 is used as analog multiplier.

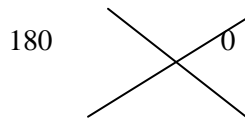
Then QPSK signal is multiplied by 'SINE & COS' carrier waves. As a result we get odd & even patterns after filtering & integrating multiplier outputs. Now by combining these two patterns we get original bit patterns. This is done by using switch.

To observe QPSK, we have given two bit patterns so that on analog CRO we can observe the wave forms. Here carrier phase changes every time ' t_b ' depending upon odd & even bit combination. It is

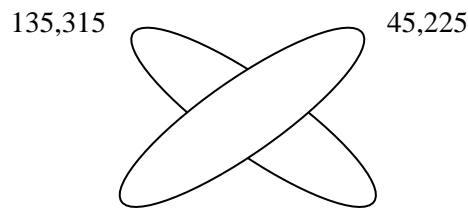
difficult to observe this on analog CRO. Details of these phase changes are shown in diagram attached. To observe QPSK we can use lissageous patterns. If we connect SINE wave to one channel & COS wave to other channel & press 'XY' button of CRO we get circle on screen.



Now if we connect SINE & its associated PSK signal to two channels & press 'XY' mode buttons we get two crossed lines.



If 'SINE' & 'QPSK' signals are connected to two channels, on 'XY' mode we get two crossed ellipses. This is because for 45, 135, 225, 315 degree we get ellipse a lissageous fig.



Also at transmitter observe that 'SINE', 'COS' wave amplitudes are lesser than resulting 'QPSK' wave because of vector addition.

We are doing this complex processing to save on bandwidth requirement of the system. This can be observed on CRO also. Observe bit pattern on CRO along with odd or even bit pattern, you will come to know that odd or even bit pattern frequency is lesser than original bit pattern frequency.

PROCEDURE:

- 1) Observe 'CLK' O/P, measure its frequency. This is nothing but 'Fb'.
- 2) Observe two patterns of pattern gen. & connect first pattern of I/P of O & E Data generator.
- 3) Observe 'O Data' & 'E Data' along with I/P pattern on DSO.
- 4) Connect 'O' Data to 'O' data pt. of 1495 Multiplier.
- 5) Connect 'E' Data to 'E' data pt. of 1495 Multiplier.
- 6) Observe 'SINE' & 'COS' waves & measure their frequencies. Also observe on 'XY' mode of DSO.
- 7) Observe pt. A with 'O Data', this is PSK of 'O Data'.
- 8) Observe pt. A with SINE wave on DSO. ('XY' mode)
- 9) Observe pt. B with 'E Data', this is PSK of 'E Data'.
- 10) Observe pt. B with COS wave on DSO. ('XY' mode)
- 11) Observe QPSK O/P with bit pattern & then with SINE wave. Press 'XY' mode & observe two ellipses.

Experiment No. 3

CO Addressed: CO2- Understand and explain various digital modulation techniques used in digital communication systems and analyze their performance in presence of AWGN noise.

AIM :-

To modulate and demodulate FSK & its spectral analysis (DSO)

EQUIPMENT: - FSK modem, DSO, connecting wires, probes.

THEORY:-

In computer peripheral & radio (wireless) communications, the binary data or code is transmitted by means of a carrier frequency that is shifted between two preset frequencies. Since a carrier frequency is shifted between two preset frequencies, the data transmission is said to use a frequency shift keying technique.

The frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the logic “0” & “1” states of the binary data signal. The frequencies corresponding to logic “1” & “0” states are commonly called as the **Mark & space** frequencies. Several standards are used to set the mark & space frequencies. For example, when transmitting teletypewriter information using MODEM system a 1070HZ-1270HZ(mark-space) pair represents the originate signal, while 2025HZ-2225HZ (mark-space) pair represents the answer signal.

In our kit we have used XR2206 IC for FSK Generation. Mark & space frequencies can be independently adjusted by the choice of timing resistors. In our kit mark frequency is fixed & space frequency can be adjusted using pot provided on panel. Detail circuit diagram is also provided. Baud rate of our system is 330HZ.

At receiver our aim is to distinguish two frequencies. For this purpose XR2211, a monolithic phase-locked Loop IC Is used. The circuit consist of a basic PLL for tracking and I/P signal within the pass-band, a quadrature phase detector which provides FSK demodulation.

PROCEDURE:-

1. Pattern “P1” or “P2” is connected as I/P to FSK Generator i.e XR2206 I/P.
2. Adjusted pot of XR2206 such that two frequencies can be easily distinguished & a neat FSK wave form is observed on DSO.

3. I/P of FSK Generator is connected to 5v i.e. (Vcc), logic “1” state & measured FSK O/P frequency, say “F1”.
4. I/P of FSK Generator is connected to GND i.e. logic “0” & observed FSK O/P, frequency say F2. Using pot of XR2206 adjusted F2 such that (f2=f1+200).
5. Calculated PLL centre frequency f₀,

$$f_0 = (f_1+f_2)/2$$
6. Then connected “A” pt. of XR2211 to “B” pt, to observe free running frequency of PLL at “D” point.
7. By using ‘VCO FREQ ADJ’ pot adjusted free running frequency to f₀.
8. Disconnected pt “A” from pt “B” & connected pt “A” to pt “C”.
9. FSK O/P is connected to I/P of capacitor near “C” pt & observe detected O/P of XR-2211 which is required O/P.

OBSERVATION TABLE:

Sr. No.	Name of Signal	Amplitude	Frequency

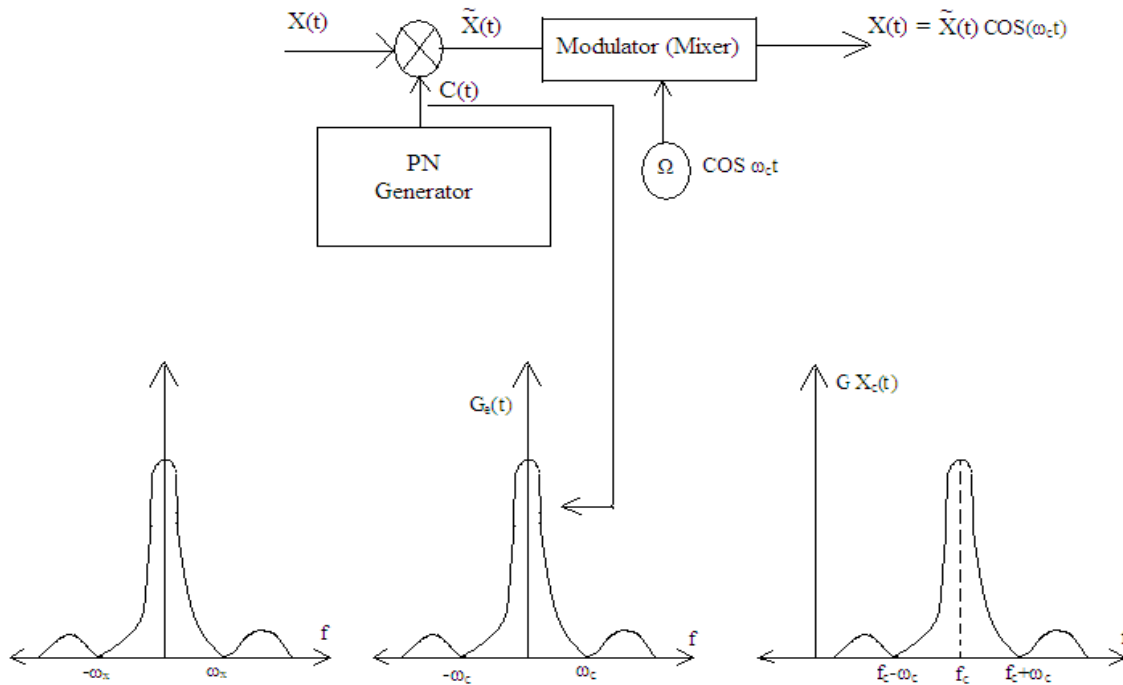
CONCLUSION:-

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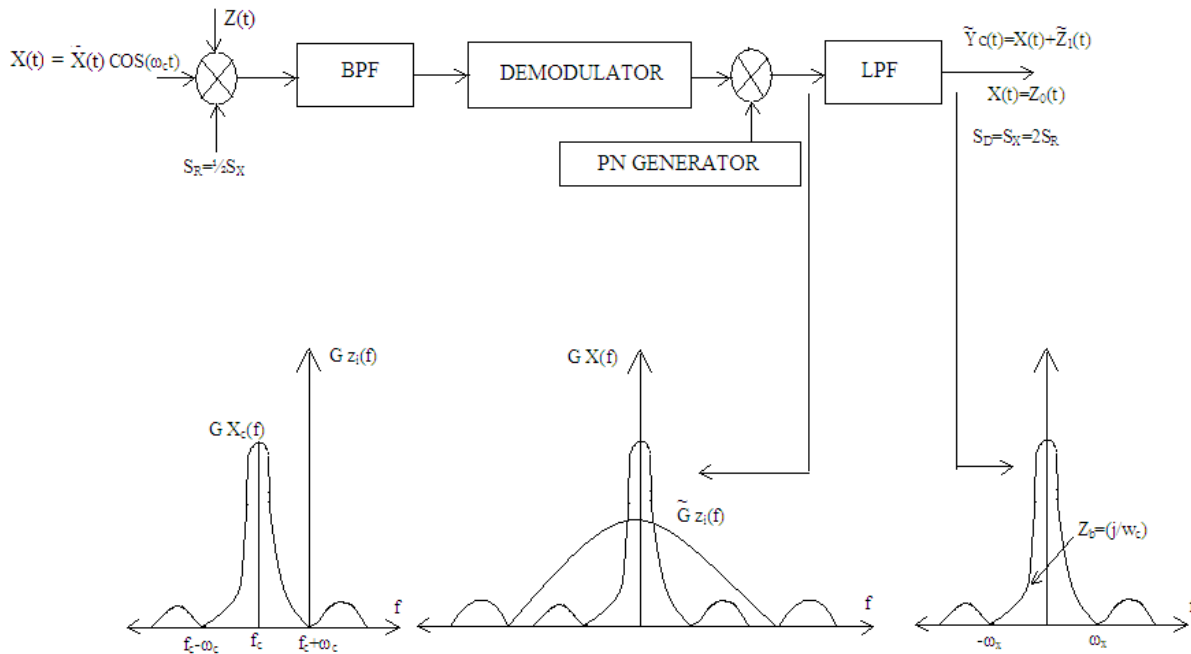
$$S_{ss} = \sqrt{(2E_s/T_s)} \times m(t)p(t) \cos(2\pi f_c t + \phi)$$

Where, $m(t)$ is data sequence $p(t)$ is pn spreading sequence f_c is the carrier frequency & is the carrier phase angle of $t=0$. Each symbol is $m(t)$ represents a data of symbol & has duration of

DS-SS TRANSMITTER



DS-SS RECEIVER



T_b . Each symbol is $m(t)$ represents a data of symbol & has a duration of T_c . The transmission of data symbols and chips coincide such that the ratio T_s to T_c is an integer. Here we notice that the higher frequency of the spreading signal $p(t)$. The resulting spread signal is then modulated using BPSK scheme. The carrier frequency f_c should have a frequency at least 5 times the chip frequency $p(t)$. In the demodulator section, we simply reverse the process. We demodulate the BPSK signal first, Low Pass Filter the signal, & then Dispread the filtered signal, to obtain the original message. The process is described by following equations:

$$M(t) = S_{ss}(t) * \cos(2\pi f_c t + Q)$$

In demodulation design, we simply reverse the process. The signal is filtered to obtain the original message.

PROCEDURE: -

- 1) Connected CRO ch1 at clock (W_k) socket & observed it.
- 2) Connected CRO ch2 at the bit clock (B_k) socket & observed it.
- 3) Connected CRO ch1 at RF carrier socket & observed the waveform.
- 4) Connected CRO ch1 NRZ data socket & observed it.
- 5) Pushed on start switch & observed PN signal.
- 6) Observed spreading signal.
- 7) Observed DS-SS signal with reference the NRZ data & spreading code signal.
- 8) Observed recovered spreading code at o/p of DS-SS modulator.
- 9) Observed the filter spreading code at o/p of LPF. Keep noise level at minimum.
- 10) Observed recovered pure NRZ data at o/p of comparator.

Experiment No. 05

CO Addressed: CO3: Describe and analyze the digital communication system with spread spectrum modulation.

AIM:- Simulation study of Performance of M-ary PSK.

EQUIPMENTS: - MATLAB software

THEORY: -

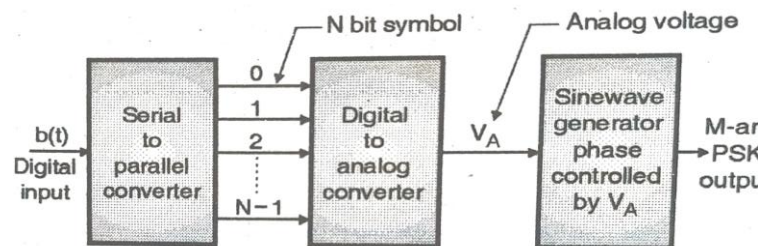
M-ary Phase Shift Keying or MPSK is a modulation where data bits select one of M phase shifted versions of the carrier to transmit the data . Thus, the M possible waveforms all have the same amplitude and frequency but different phases. The signal constellations consists of M equally spaced points on a circle

Generation : Group 'N' successive bits together to form N bits symbol.Each symbol will extend over a period of $N T_b$ where T_b is the duration of one bit. Due to grouping we have $2^N=M$ symbols.These M symbols are represented by sinusoidal signals of duration $T_s=NT_b$ having phase shift of $2 \pi/M$ radians. Thus the M-ary PSK waveform can be mathematically represented as

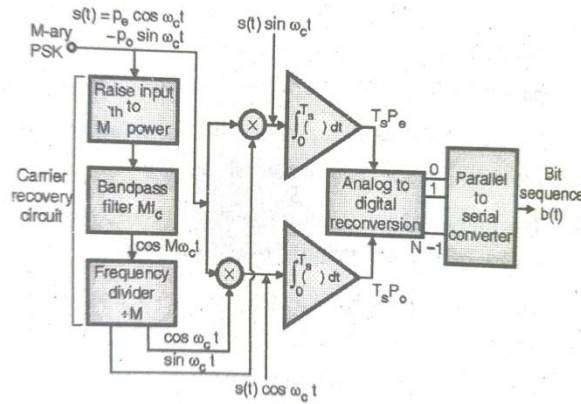
$$V_{M\text{-ary}} = \sqrt{2P_s} \cos(\omega_c t + \phi_m) \quad \text{where } m=0,1,2,\dots,(M-1) ; \quad \phi_m=(2m+1)\frac{\pi}{M}$$

M-ary PSK Transmitter :

The bit stream $b(t)$ is applied to serial to parallel converter. This can store N bits of symbol. Output of serial to parallel converter remains unchanged for NT_b duration. N bit output is then applied to D/A converter. This N bits are converted into an analog signal V. D/A converter can have $2^N=M$ number of distinct values , corresponding to the M symbols. Finally this analog voltage is applied to a sinusoidal signal generator ,which produces constant amplitude sinusoidal output voltage , the phase ϕ_m of which has one to one correspondence to N bit symbols. The phase will change once per symbol time $T_s=NT_b$. Thus M-ary PSK is generated



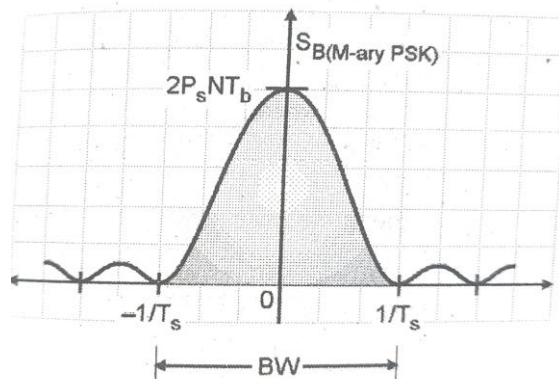
M-ary PSK Receiver :

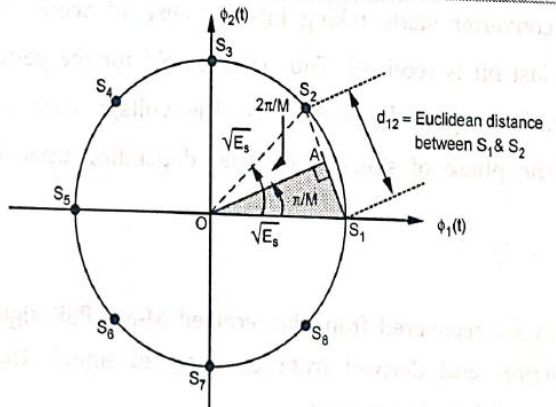


The M-ary receiver works on principle of synchronous demodulation as in BPSK and QPSK. The carrier recovery system will require a device which can raise received signal to M^{th} power. This signal is then applied to band pass filter. At filter output we get sinusoidal signal at frequency Mf_c i.e M^{th} harmonic of f_c . The frequency is then divided by M to obtain carrier at frequency f_c . Two carriers produced at filter output are $\cos \omega_c t$ and $\sin \omega_c t$ which are applied to two multipliers. The other input to multiplier is connected to received M-ary PSK signal. Output is then given to integrators. Since M-ary PSK is non-offset type system, integrators will extend integration over same time interval. The outputs of integrators are proportional to $T_s p_e$ and $T_s p_o$ respectively and they change symbol rate. output is connected to A to D converter which yields N bit transmitted signal. These signal is converted into $b(t)$ using parallel to serial converter. Now the operating systems with $N=4$ and $M=16$ are common.

$$\text{BandWidth} = \frac{2f_b}{N} = \frac{2f_b}{4} = \frac{f_b}{2}$$

$$S_{B(M\text{-ary PSK})}(f) = 2P_s N T_b \left(\frac{\sin(\pi f N T_b)}{\pi f N T_b} \right)^2$$





CONCLUSION: -

Staff Signature

Experiment No. 06

CO Addressed: CO3: Describe and analyze the digital communication system with spread spectrum modulation.

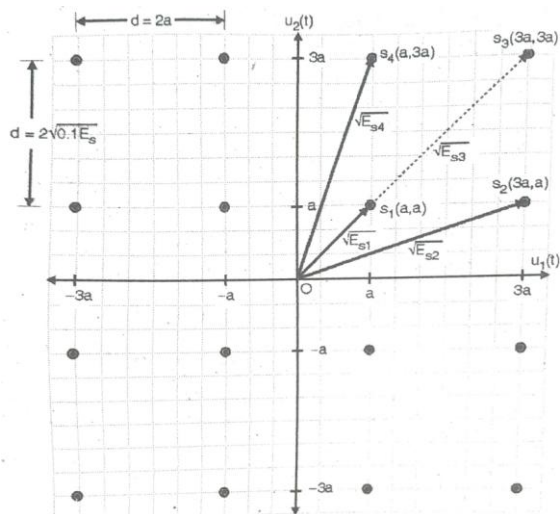
AIM:- To study the theory of QASK (Quadrature Amplitude Shift Keying).

EQUIPMENTS: - DSO, patch cords, probes

THEORY: -

Symbols transmitted using BPSK, QPSK or M-ary PSK are of same amplitude. Also noise immunity will improve if the signal vector differ not only in phase but also in amplitude. Such a system is called amplitude and phase shift keying system. In this system the direct modulation of carriers in quadrature is involved, therefore this system is called as quadrature amplitude phase shift keying

Let us assume that using QASK we want to transmit a symbol consisting of 4 bits. That means $N=4$ and there are 16 different possible symbols. Hence the QASK system should be able to generate 16 different distinguishable signals . A possible geometric representation of 16 signals is as shown



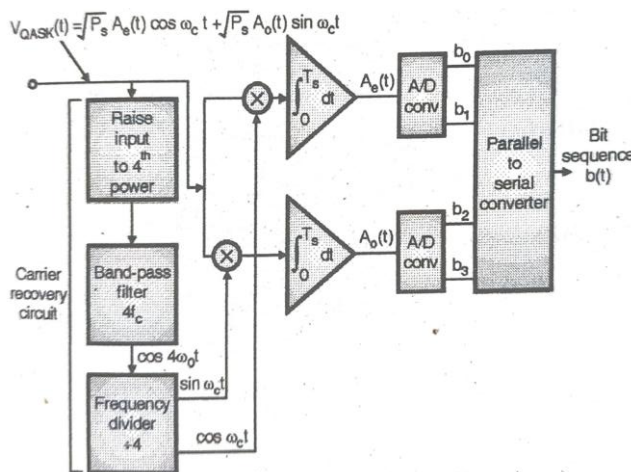
QASK Transmitter :

The bit stream $b(t)$ is applied to a serial to parallel converter operating on a clock which has period of T_s sec. the four signals are b_{k+3} , b_{k+2} , b_{k+1} , b_k . out of these four bits first two are

applied to first D/A converter and other two to second D/A converter. output of first converter is $A_e(t)$ used to modulate carrier $\sqrt{P_s} \cos \omega_c t$ and second converter gives $A_o(t)$ used to modulate $\sqrt{P_s} \sin \omega_c t$ with help of balanced modulators. balanced modulators outputs are added together to get QASK signal which is expressed as

$$V_{QASK} = A_e(t) \sqrt{P_s} \cos(\omega_c t) + A_o(t) \sqrt{P_s} \sin(\omega_c t)$$

QASK Receiver :



Like QPSK this is also synchronous demodulation which requires locally generated set of quadrature carriers(90 phase shift). The input QASK signal is first raised to fourth power and using band pass filter with centre frequency $4f_c$ alongside with frequency divider($\div 4$). i.e

$$V_{QASK}^4(t) = [P_s]^2 [A_e(t) \cos(\omega_c t) + A_o(t) \sin(\omega_c t)]^4$$

Then passed through BPF with freq. $4f_c$ so we neglect all other terms except which have freq $4f_c$

$$V_{QASK}^4(t) = \frac{P_s}{8} [A_e^4(t) + A_o^4(t) - 6A_e^2(t) A_o^2(t)] \cos 4\omega_c t + \frac{P_s}{2} [A_e(t) + A_o(t)] [A_e^2(t) - A_o^2(t)] \sin 4\omega_c t$$

The two balanced modulators are used with two integrators to recover the signals $A_e(t)$ and $A_o(t)$. Both integrate over period T_s . Finally the original bits are obtained from $A_e(t)$ and $A_o(t)$

By using A/D converters .outputs of converters are applied to serial to parallel converter to obtain sequence $b(t)$

$$BW = f_s - (-f_s) = 2 f_s = \frac{2}{T_s} = \frac{2}{NT_b}$$

CONCLUSION: -

Staff Signature

EXPERIMENT NO: 7

Aim: Simulation study of OFDM transmitter and receiver.

CO Addressed: CO3- Describe and analyze the digital communication system with spread spectrum modulation.

Theory: The set of 4G wireless standards is based on the revolutionary new technology of Orthogonal Frequency Division Multiplexing (OFDM). Orthogonal Frequency Division Multiplexing forms the basis of fourth generation wireless communication systems. OFDM is used in 4G wireless cellular standards such as Long Term Evolution (LTE) and WiMAX (Worldwide Interoperability for Microwave Access). OFDM is a keyword broadband wireless technology which supports data rates in excess of 100 Mbps. OFDM is a combination of modulation and multiplexing. In this technique, the given resource (bandwidth) is shared among individual modulated data sources. The multiple access technology based on OFDM is termed Orthogonal Frequency Division for Multiple Access (OFDMA).

Necessity of OFDM:

OFDM is very effective for communication over channels with frequency selective fading (different frequency components of the signal experience different fading). It is very difficult to handle frequency selective fading in the receiver, in which case, the design of the receiver is hugely complex. Instead of trying to mitigate frequency selective fading as a whole (which occurs when a huge bandwidth is allocated for the data transmission over a frequency selective fading channel), OFDM mitigates the problem by converting the entire frequency selective fading channel into small flat fading channels (as seen by the individual subcarriers). Flat fading is easier to combat (when compared to frequency selective fading) by employing simple error correction and equalization schemes.

An OFDM system is defined by IFFT/FFT length – N , the underlying modulation technique (BPSK/QPSK/QAM), supported data rate, etc. The FFT/IFFT length N defines the number of total subcarriers present in the OFDM system.

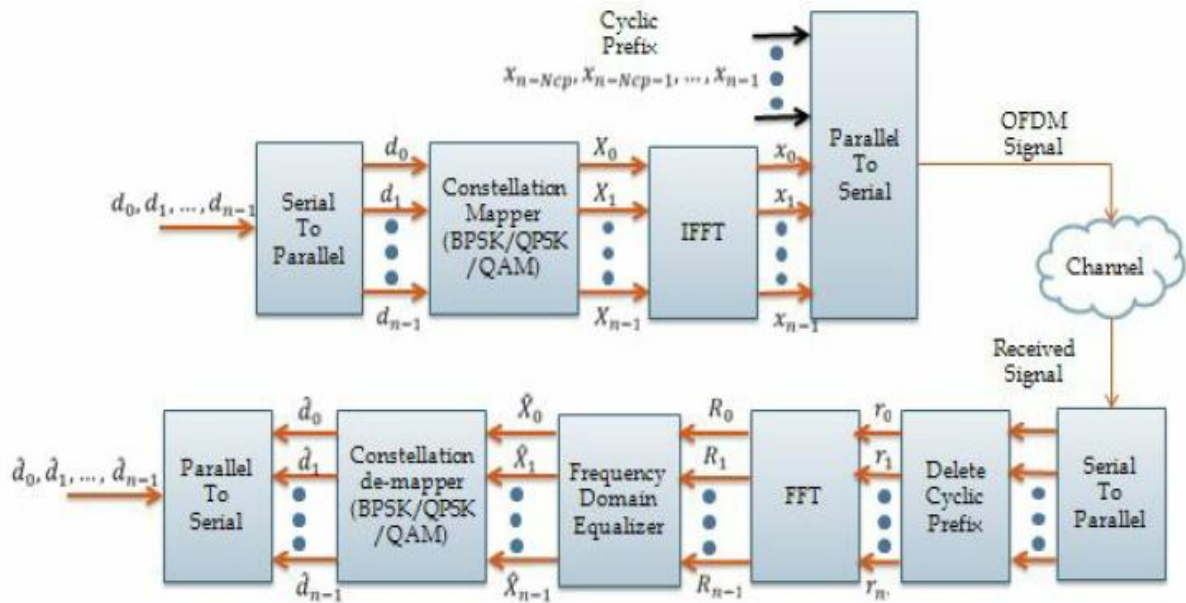


Fig. 1 Model for simulating the OFDM system

In the figure, symbols represented by small case letters are assumed to be in time domain, whereas the symbols represented by uppercase letters are assumed to be in frequency domain. Consider data bits $D = \{d_0, d_1, d_2, \dots\}$. Select number of subcarriers required to send the given data. As a generic case, assume N subcarriers. The data (D) is first converted from serial stream to parallel stream depending on the number of sub-carriers (N). Decide digital modulation techniques such as BPSK/ QAM. Apply IFFT algorithm on generated symbols and add cyclic prefix bits. Finally, the resultant output from the N parallel arms are summed up together to produce the OFDM signal. The channel in this case is modeled as a simple AWGN channel. Since the channel is considered to be an AWGN channel, there is no need for the frequency domain equalizer in the OFDM receiver as shown in Fig. 1. Reverse the process at the receiver side. Compare the transmitted and received bits to compute bit error rate.

CONCLUSION: -

Signature:-

EXPERIMENT NO: 8

TITLE: Simulation study of various Entropies and mutual information in a communication system

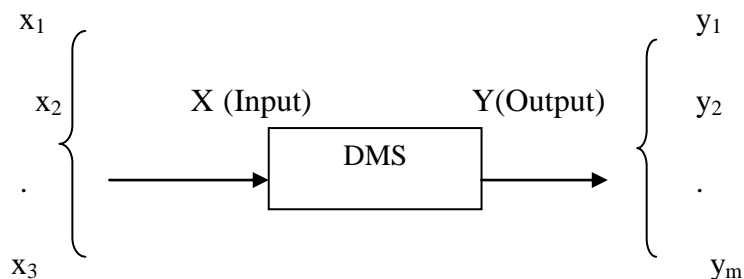
CO Addressed: CO4- Analyze a communication system using information theoretic approach.

THEORY:

Discrete Communication Channel (DCC)

Channel Representation:

A communication channel is the path or medium through which the symbols flow to the receiver. A discrete channel (DMC) is a statistical model with an input X and an output Y. During each unit of the time (signaling interval), the channel accepts an input symbol from X, and in response it generates an output symbol from Y. The channel is “**discrete**” when the alphabets of X and Y are both finite. It is “**Memory-less**” when the current output depends on only the current input and not on any of the previous inputs.



A diagram of a DMC with m inputs and n outputs. The input X consists of input symbols $x_1, x_2, x_3, \dots, x_m$. The a priori probabilities of these source symbols $P(x_i)$ are assumed to be known. The output Y consists of output symbols y_1, y_2, \dots, y_n .

Channel Matrix:

Channel Transition Probability

Each possible input-to-output path is indicated along with a conditional probability $P(y_j/x_i)$, where $P(y_j/x_i)$ is the conditional probability of obtaining output y_j given that the input is x_i , and is called channel transition probability.

A channel is completely specified by the complete set of transition probabilities.

$$[P(Y/X)] = \begin{pmatrix} P(y_1/x_1) & P(y_2/x_1) & \dots\dots & P(y_n/x_1) \\ P(y_1/x_2) & P(y_2/x_2) & \dots\dots & P(y_n/x_2) \\ \cdot & \cdot & \cdot & \\ \cdot & \cdot & \cdot & \\ P(y_1/x_m) & P(y_2/x_m) & \dots\dots\dots & P(y_n/x_m) \end{pmatrix} \text{ m}^* \text{n}$$

Matrix of channel transition probabilities i.e. $[P(Y/X)]$ is called the channel matrix.

Important property of $[P(Y/X)]$ matrix: Since each input to the channel results in some output, each row of the channel matrix must sum to unity, that is

$$\sum_{j=1}^n p\left(\frac{y_j}{x_i}\right) = 1 \text{ for all } i$$

Mutual Information

Mutual information is the net amount of information that passes through the discrete communication channel. The mutual information $I(X;Y)$ of a channel is defined by

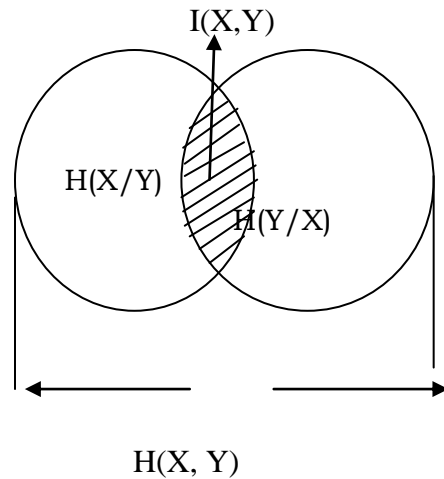
$$I(X; Y) = H(X) - H(X/Y) \text{ bits/ Symbol}$$

We know that in DCC, the channel output Y is a noisy version of the channel output. Where $H(X)$ represents the uncertainty about channel input before the channel output is observed and

$H(X/Y)$ represents the uncertainty about the channel input after the channel output is observed. The difference $H(X) - H(X/Y)$ must represent our uncertainty about channel input that is resolved by observing the channel output. This important quantity is called mutual information and is represented by $I(X;Y)$.

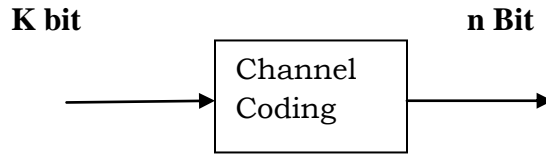
Properties of mutual information:

- (a) Mutual information is always symmetric, i.e. $I(X;Y) = I(Y;X)$
- (b) Mutual information is always nonnegative, $I(X;Y) \geq 0$
- (c) Mutual information of a channel is related to the joint entropy of the channel input and channel output by equation $I(X;Y) = H(X) + H(Y) - H(X,Y)$



Channel Coding: Channel coding consist of mapping the incoming data sequence into a channel input sequence and inverse mapping the channel output sequence into an output data sequence in such a way that the overall effect of channel noise on the system is minimized. The first mapping operation is performed in the transmitter by a channel encoder, whereas the inverse mapping operation is performed in the receiver by a channel decoder.

The channel encoder and channel decoder are both under the designer's control and should be designed to optimize reliability of the communication system. The approach taken is to introduce redundancy in the channel encoder so as to reconstruct the original source sequence as accurately as possible. We may view channel coding as the dual of source coding in that former introduces controlled redundancy to improve reliability, whereas the latter reduces to improve efficiency.

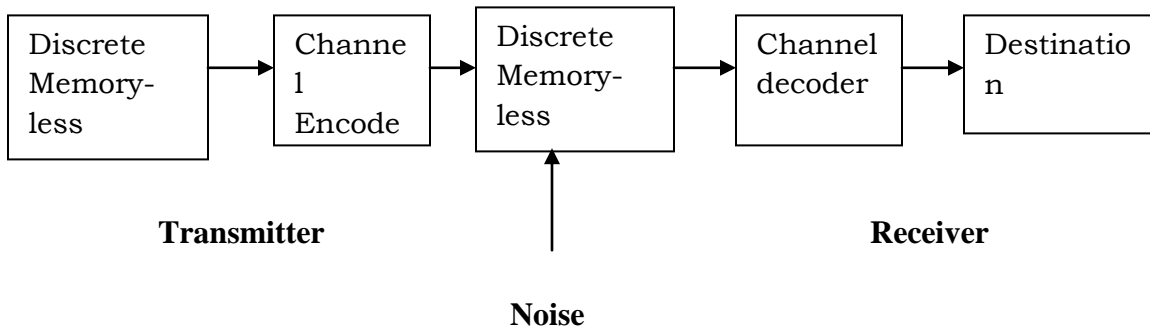


The number of redundant bits added by the encoder to each transmitted block is $n-k$ bits. The ratio k/n is called the code rate and is denoted by r . where r is code rate and is less than unity.

The accurate reconstruction of the original source sequence at the destination requires that the average probability of symbol error be arbitrarily low. This raises the following important question: does there exist a channel coding scheme such that the probability that a message bit will be in error is less than any positive number ϵ (i.e., as small as we want it), and yet the channel coding scheme is efficient in that the code rate need not be small. The answer to this fundamental question is an emphatic “Yes”. Indeed, the answer to the question is provided by Shannon’s second theorem in terms of the channel capacity C_s .

Consider DMS, has the source alphabet x and entropy $H(x)$ bits per source symbol. If the source emits symbols once every T_s seconds. Hence, the average information rate of the source is $H(x)/T_s$ Seconds. The decoder delivers decoded symbols to the destination from the source alphabet x and at the same source rate of one symbol every T_s Seconds.

The discrete memory less channel has a channel capacity equal to C_s bits per use of the channel. We assume that the channel is capable of being used once every T_c Seconds. Hence, the channel capacity per unit time is C_s/T_c bits per second, which represents the maximum rate of information transfer over the channel.



error tends to zero as the length of the code increases, again provided that the condition is satisfied.

Important Formulae:

1) $P(x_i) = \{p(x_1), p(x_2), p(x_3) \dots p(x_i) \dots p(x_m)\}$

2) $P(y_j) = \{p(y_1), p(y_2), p(y_3) \dots p(y_j) \dots p(y_n)\}$

3) $P(x_i, y_j) = P(x_i/y_j) \cdot p(y_j)$
 $= P(y_j/x_i) \cdot p(x_i)$

4) $H(X) = \sum_{i=1}^m P(X_i) \log_2(1/P(X_i))$

5) $H(Y) = \sum_{j=1}^n P(Y_j) \log_2(1/P(Y_j))$

6) $H(X, Y) = \sum_{i=1}^m \sum_{j=1}^n P(X_i, Y_j) \log_2(1/P(X_i, Y_j))$

7) $H\left(\frac{X}{Y}\right) = \sum_{i=1}^m \sum_{j=1}^n P(x_i, y_j) \log(1/(P(x_i/y_j)))$

8) $H\left(\frac{Y}{X}\right) = \sum_{i=1}^m \sum_{j=1}^n P(x_i, y_j) \log(1/(P(y_j/x_i)))$

9) $H(X, Y) = H\left(\frac{X}{Y}\right) + H(Y)$

10) $H(X, Y) = H\left(\frac{Y}{X}\right) + H(X)$

11) $I(X, Y) = H(X) - H\left(\frac{X}{Y}\right)$ or $I(X, Y) = H(Y) - H\left(\frac{Y}{X}\right)$

12) $I(X, Y) = H(X) - H\left(\frac{X}{Y}\right)$ or $I(X, Y) = H(Y) - H\left(\frac{Y}{X}\right)$

13) $I(X, Y) = \sum_{i=1}^m \sum_{j=1}^n P(X_i, Y_j) \log_2(P(X_i/Y_j)/P(x_i))$

14) $I(y, x) = \sum_{i=1}^m \sum_{j=1}^n P(X_i, Y_j) \log_2(P(y_j/x_i)/P(y_i))$

15) $P(x_i) = \sum_{j=1}^n P(x_i, y_j)$

16) $P(y_j) = \sum_{i=1}^m P(x_i, y_j)$

Algorithm

1. Read out the channel matrix from the user.

Read out m & n from the user. Where,

m- no. of inputs to DMC. (No of rows of channel Matrix)

n-no. of outputs of DMC.(No. of columns of channel matrix)

2. Read out elements of the channel matrix (transition probabilities).
3. Identify the type of matrix.
 - If it is joint probability matrix, then addition of all elements should be equal to 1.
 - If it is not joint probability matrix then there is a possibility of conditional probability P(Y/X) either P(X/Y).
 - If it is a conditional P(Y/X) then individual row wise addition must be 1.
 - If individual column wise addition is 1, then it is P(X/Y) matrix. Finally print the matrix.
4. If the matrix is joint probability matrix go to next step. But if matrix is conditional then convert it into joint probability matrix.
 - If matrix is P(Y/X) then take input probability distribution from user P(X₀), P(X₁), P(X₂),.....P(X_{m-1}).

$$\sum_{i=0}^{m-1} p(x_i) = 1$$

& after that you multiply P(X₀) to the first row of P(Y/X) & second row of P(Y/X) to the P(X₁). Similarly multiply (m-1)th row of P(Y/X) to the P(X_{m-1}).

Resultant matrix is joint probability matrix.

- If matrix is P(X/Y) then take P(Y₀), P(Y₁), P(Y₂),.....P(Y_{n-1}) from user. Multiply first column with P(Y₀), second column with P(Y₁), & last column with P(Y_{n-1}) & resultant matrix is P(X, Y).
5. If the matrix is joint probability matrix, the row wise addition of joint probability matrix is P(X₀), P(X₁), .P(X_{m-1}). & column wise addition of joint probability matrix is P(Y₀), P(Y₁),.....P(Y_{n-1}).
 6. By using P(X) value calculates H(X).

$$H(X) = \sum_{i=0}^{m-1} P(X_i) \log_2(1/P(X_i))$$

By using P(Y) values calculate H(Y).

$$H(Y) = \sum_{j=0}^{n-1} P(Y_j) \log_2(1/P(Y_j))$$

After calculating $H(X)$ & $H(Y)$ which is a transmission (input)

& reception (output) entropies, calculate joint entropy.

$$H(X, Y) = \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} P(X_i, Y_j) \log_2(1/P(X_i, Y_j))$$

7. Calculation of conditional entropies:

- $H(X, Y) = H\left(\frac{X}{Y}\right) + H(Y)$
- $H\left(\frac{X}{Y}\right) = H(X, Y) - H(Y)$
- $H(X, Y) = H\left(\frac{Y}{X}\right) + H(X)$
- $H\left(\frac{Y}{X}\right) = H(X, Y) - H(X)$

8. Calculation for mutual information:

$$I(X, Y) = H(X) - H\left(\frac{X}{Y}\right) \text{ or } I(Y, X) = H(Y) - H\left(\frac{Y}{X}\right)$$

9. Channel capacity:

$$C_s = \max_{\{P(X_i)\}} I(X, Y)$$

Maximization of mutual information is called Channel capacity C_s , where maximization is possible on probability distribution $P(X) = \{P(X_0), P(X_1), \dots, P(X_{m-1})\}$

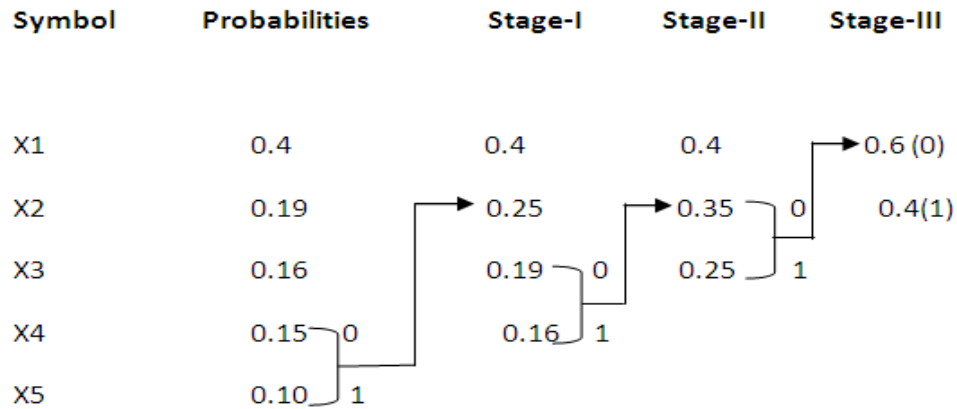
&

$$\sum_{i=0}^{m-1} P(X_i) = 1$$

10. Read out the channel rate from the user. $r_c = 1/T_c$ no. of symbols/sec. Where r_c is no. of symbol transmitted (passes) by the Communication channel

$$C = r_c * C_s = C_s/T_c$$

Conclusion:-



Symbol	Probabilities	Source code	Source code Length (l_k)
X1	0.4	1	1
X2	0.19	000	3
X3	0.16	001	3
X4	0.15	010	3
X5	0.10	011	3

$$H(X) = 2.3125$$

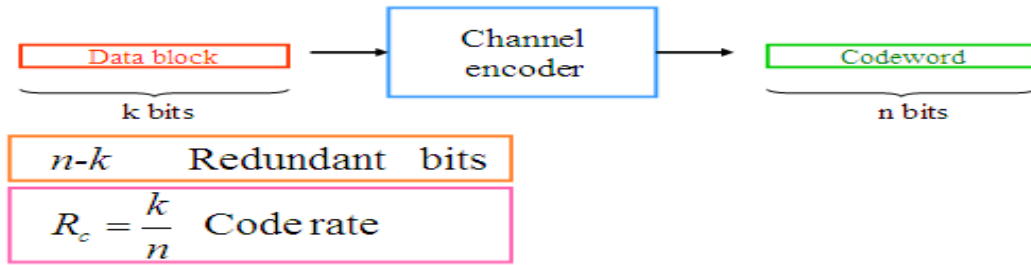
$$\bar{L} = 2.3125$$

$$\% n = H(X) / \bar{L} \times 100$$

$$n = 100\%$$

- Perform the practical to evaluate variable length source coding using Huffman coding using C Programming or Matlab.

Huffman Encoding Algorithm



Generator Matrix:

- The Generator matrix provides a concise and efficient way of representing a linear block code. The generator matrix converts (encodes) a vector of length k to a vector of length n . The generator matrix will be $k \times n$ matrix with rank k .

$$G = [I_{k \times k} \quad P_{k \times (n-k)}]_{k \times n}$$

Where I is identity matrix size is $k \times k$, P is parity matrix and size is $k \times (n-k)$, Size of G matrix is $k \times n$

Systematic block code (n,k)

For a systematic code, the first (or last) k elements in the codeword are information bits.

Encoding in (n,k) block code

- $C = mG$ or dG
 - Where c is called the codeword and d or m is called the information word.
 - Where C is $1 \times n$ vector, d is $1 \times k$ vector and G is generator matrix.
 - $C = (c_1, c_2, \dots, c_n) = (m_1, m_2, \dots, m_k \quad p_1, p_2, \dots, p_{n-k})$.
- Note: Mod 2 arithmetic: Multiplication similar to AND operation, addition (subtraction) similar to EX-OR operation.

Linear Block Coding Example:

Consider (7,4) LBC with the generator matrix

$$G = \begin{matrix} 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 \end{matrix}$$

0 0 0 1 1 0 1

Find out all possible code vectors ,error detection & correction capability

Message Word (Length k bits)	Code Vector C = mG (Length n bits)	Weight of code vectors (Wc)	Remarks
0000	0000000	0	Zero Code Vector
0001	0001101	3	All remaining code vectors are non zero Code vector. d_{\min} = Minimum weight of non zero code vector = 3 (All these code vector are transmitted by transmitter it is also called valid code vector and it is equal to 2^k , where k is message length)
0010	0010111	4	
0011	0011010	3	
0100	0100011	3	
0101	0101110	4	
0110	0110100	3	
0111	0111001	4	
1000	1000110	3	
1001	1001011	4	
1010	1010001	3	
1011	1011100	4	
1100	1100101	4	
1101	1101000	3	
1110	1110010	4	
1111	1111111	7	

Minimum Distance: d_{\min} = Minimum weight of non zero code vectors =3

Error Detection Capabilities of code $t_d \leq d_{\min} - 1 = 2$

Error Correction Capabilities of code $t_c \leq (d_{\min} - 1)/2 = 1$

Algorithm of Linear Block Coding:

- a. Read out the message length (k) and code vector length(n)
- b. Read out the parity matrix (P).
- c. Construct G matrix.
- d. Find out all possible messages.
- e. Find out all possible code vector generated by encoder (valid code vector) $C = d \times G$
- f. Find out weight of individual code vector (Wc)
- g. Calculate d_{\min} , Error detection capability and Error correction capability of the code.

Linear block decoding (minimum distance consideration)

Decoding is the process of detecting and correcting errors, when message in the form of code words are transmitted over noisy channel. How many errors can be detected and corrected? The answer of above question is it will depend on the design of the code. The number of errors, code can detect or correct is called error detecting and error correcting capability of the code

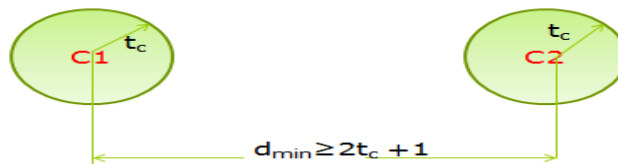
Error Detection

As long as one code word is not transformed into another valid codeword, we can detect whether there was an error in transmission or not. One valid code word is transformed into another valid code word after distance d_{min} . Thus the number of errors can be detected depends on d_{min} . $t_d \leq (d_{min}-1)$ where t_d is error detection capability of the code.

Error Correction:

In two cases an error correction is not possible.

- If the received code vector is near to another valid code vector (which is not transmitted) then there is wrong decoding.
- If received codeword might be at same distance from two or more valid code vectors, it is then not possible to correct the code.



$t_c \leq (d_{min}-1)/2$
where t_c is small integer

Consider a code c with minimum distance $d_{min} \geq 2t_c + 1$. The spheres of radius t_c centered at the codeword's $\{ c_1, c_2, c_3, \dots, C_m \}$ of c will then be disjoint.

- **Decoding Process** → Any received vector can be represented as a point in this space . If this point lies within a sphere, then by nearest neighbor decoding it will be decoded as the center of the sphere.

If t_c or fewer error occur the received word will definitely lie within the sphere of the codeword that was transmitted, and will be correctly decoded.

If however, larger than t_c errors occur, it will escape the sphere, thus resulting in incorrect decoding.

Important Note: Linear Block Decoding

- If the multiplication of the received word (at the receiver) with the transpose H yields a non-zero vector, it implies that error has occurred.
 - This methodology, however will fail if the errors in the transmitted codeword exceed the number of errors for which the coding scheme is designed.

Numerical Example:

Consider the previous example

Prepare error decoding table (look up table)

If the received code vector is 1111110, find out corrected code vector.

Error Decoding Table:

Bit in Error	Single Bit Error	Syndrome Vector
	Pattern	
	E1 E2 E3 E4 E5 E6 E7	$S = EH^T$
1 st Bit in Error	1 0 0 0 0 0 0	1 1 0
2 nd Bit in Error	0 1 0 0 0 0 0	0 1 1
3 rd Bit in Error	0 0 1 0 0 0 0	1 1 1
4 th Bit in Error	0 0 0 1 0 0 0	1 0 1
5 th Bit in Error	0 0 0 0 1 0 0	1 0 0
6 th Bit in Error	0 0 0 0 0 1 0	0 1 0
7 th Bit in Error	0 0 0 0 0 0 1	0 0 1

If the received code vector $R = 1111110$, then syndrome of received code vector is $RH^T = 001$.

